AMENDMENTS TO THE SPECIFICATION

Please amend paragraph 27 to read as follows:

[0027] Turning now to **Figure 2**, a series of output queues **202**, **204**, **206**, ~~and~~**208** and **208** are provided. Each of output queues **202**, **204**, **206**, ~~and~~**208** and **208** is associated with a particular priority level. In this example, four priority levels, numbered 0-3, are depicted, with 0 being the lowest priority and 3 being the highest priority. Each of output queues **202**, **204**, **206**, ~~and~~**208** and **208** receives only those packets from input queue **102** that have a priority that matches the priority of that particular output queue. For example, since output queue **206** is associated with priority level 2, output queue **206** will receive only those packets from input queue **102** that have a priority level of 2.

Please amend paragraph 28 to read as follows:

[0028] Packet selection logic **218** has the responsibility of picking the next packet from output queues **202**, **204**, **206**, ~~and~~**208** and **208** to submit to port **220** for transmission. In order to give meaning to the priority scheme, packet selection logic **218** picks the highest priority packet contained in one of output queues **202**, **204**, **206**, ~~and~~**208** and **208**. Alternatively stated, a packet may not be selected for transmission on port **220** unless there are no higher-priority packets available (on the higher-priority output queues).

Please amend paragraph 29 to read as follows:

[0029] Each of output queues **202**, **204**, **206**, ~~and~~**208** and **208** outputs a full indicator signal (signals **210**, **212**, **214**, ~~and~~**216** and **216**, respectively) that, when asserted, indicates that its respective output queue is full. Thus, for example, when output queue **202** is full, output queue **202** asserts full indicator signal **210**. Full indicator signals **210**, **212**, **214**, ~~and~~**216** and **216** form the inputs to a nor gate **222**, which outputs "ready" signal **106** to read control **104** (in **Figure 1**).

Please amend paragraph 30 to read as follows:

[0030] The result of this arrangement is that a packet may not leave input queue **102** if any of the output queues at the destination port (output queues **202**, **204**, **206**, ~~and~~**~~208~~** and **208**) is full. Thus, when a packet leaves input queue **102**, there must be at least one space available on each of output queues **202**, **204**, **206**, ~~and~~**~~208~~** and **208** at the destination port. This ensures that space will quickly become available to accept whatever priority packet is waiting at the head of the input queue.

Please amend paragraph 32 to read as follows:

[0032] Turning now to **Figure 4**, a series of output queues **402**, **404**, **406**, ~~and~~**~~408~~** and **408** are provided. As in the embodiment depicted in **Figure 2**, each of output queues **402**, **404**, **406**, ~~and~~**~~408~~** and **408** is associated with a particular priority level. Each of output queues **402**, **404**, **406**, ~~and~~**~~408~~** and **408** receives only those packets from input queue **302** that have a priority that matches the priority of that particular output queue.

Please amend paragraph 33 to read as follows:

[0033] Packet selection logic **418** has the responsibility of picking the next packet from output queues **402**, **404**, **406**, ~~and~~**~~408~~** and **408** to submit to port **420** for transmission. As with the embodiment described in **Figure 2**, packet selection logic **418** packs the highest-priority packet contained in one of output queues **402**, **404**, **406**, ~~and~~**~~408~~** and **408**.

Please amend paragraph 34 to read as follows:

[0034] As in **Figure 2**, each of output queues **402**, **404**, **406**, ~~and~~**~~408~~** and **408** outputs a full indicator signal (signals **410**, **412**, **414**, ~~and~~**~~416~~** and **416**, respectively) that, when asserted, indicates that its respective output queue is full. However, unlike the embodiment in **Figure 2**, which fed indicator signals **210**, **212**, **214**, ~~and~~**~~216~~** and **216** into nor gate **222**, full indicator signals **410**, **412**, **414**, ~~and~~**~~416~~** and **416** form the input to a packet accept logic circuit **422**, which also accepts priority indicator **308** as an input.

Packet accept logic circuit **422** asserts its "ready" signal output **306** if and only if either 1.) there are no full output queues (*i.e.,* none of full indicator signals **410**, **412**, **414**, ~~and~~**~~416~~** and **416** are asserted) or 2.) the priority indicated by priority indicator **308** from the source input port is less than the priority of the highest-priority output queue that is full.

Please amend paragraph 36 to read as follows:

[0036] The result of this arrangement is that a packet may not leave queue **102** if it has a priority that is higher than the priority of a full output queue. This strategy can potentially relieve the blocking of high-priority packets at input queue **302** more quickly than that depicted in **Figure 1** and **Figure 2**, since any lower-priority packets that are at the head of input queue **302** can potentially be moved out of the way more quickly. The logic required to implement this second preferred embodiment is somewhat more complex than that for the first embodiment, however, since additional logic circuitry is required to produce priority indicator **308** and to interpret priority indicator **308** and full indicator signals **410**, **412**, **414**, ~~and~~**~~416~~** and **416** (*i.e.,* packet accept logic **422**).